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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,693	12/11/2003	Wayne A. Britson	ROC920030248US1	8659

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EXAMINER	
RIZK, SAMIR WADIE	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,693	BRITSON ET AL.	
	Examiner	Art Unit	
	Sam Rizk	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/11/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTIONS

- Claims 1-20 have been submitted for examination
- Claims 1-20 have been rejected

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Garreau US patent no. 6425101 (Hereinafter Garreau).

3. In regard to claim 1, Garreau teaches:

- A method for testing an integrated circuit (IC) comprising:

(Note: Abstract in Garreau))

- employing one of a plurality of input lines to receive a test signal for a processor;

(Note: FIG. 4, reference characters (400) Programmable Switch in Garreau)

- employing one of a plurality of output lines to send a test result from the processor; and

(Note: FIG. 4, reference characters (400) Programmable Switch in Garreau)

- if the test result is unsuccessful, performing at least one of:
- employing a remaining one of the plurality of input lines to receive the test signal for the processor; and

(Note: col. 6, lines (49-67) through col. 7, lines (1-28) in Garreau)

- employing a remaining one of the plurality of output lines to send the test result from the processor.

(Note: col. 6, lines (49-67) through col. 7, lines (1-28) in Garreau)

4. In regard to claim 2, Garreau teaches:

- The method of claim 1 wherein employing one of the plurality of input lines to receive the test signal for the processor includes:
- applying the test signal to each of the plurality of input lines;
- selecting one of the plurality of input lines; and
- receiving the test signal for the processor from the selected input line.

(Note: FIG. 4, reference characters (400) Programmable Switch in Garreau)

(Note: col. 6, lines (49-67) through col. 7, lines (1-28) in Garreau)

5. In regard to claim 3, Garreau teaches:

- The method of claim 1 wherein employing one of the plurality of output lines to send the test result from the processor includes:
- applying the test result to each of the plurality of output lines;
- selecting one of the plurality of output lines; and
- sending the test result from the processor using the selected output line.

(Note: FIG. 4, reference characters (400) Programmable Switch in Garreau)

(Note: col. 6, lines (49-67) through col. 7, lines (1-28) in Garreau)

6. In regard to claim 4, Garreau teaches:

- The method of claim 1 wherein employing a remaining one of the plurality of input lines to receive the test signal for the processor includes:
- selecting a remaining one of the plurality of input lines; and
- employing the selected remaining one of the plurality of input lines to receive the test signal.

(Note: FIG. 4, reference characters (400) Programmable Switch in Garreau)

(Note: col. 6, lines (49-67) through col. 7, lines (1-28) in Garreau)

7. In regard to claim 5, Garreau teaches:

- The method of claim 4 wherein selecting a remaining one of the plurality of input lines includes:

- modifying a first select signal; and
- selecting a remaining one of the plurality of input lines based on the modified first select signal.

(Note: col. 4, lines (57-67) through col. 5, lines (1-25) the Master controller detail description in Garreau)

8. In regard to claim 6, Garreau teaches:

- The method of claim 1 wherein employing a remaining one of the plurality of output lines to send the test result from the processor includes:
- selecting a remaining one of the plurality of output lines; and
- employing the selected remaining one of the plurality of output lines to send the test result from the processor.

(Note: FIG. 4, reference characters (400) Programmable Switch in Garreau)

(Note: col. 6, lines (49-67) through col. 7, lines (1-28) in Garreau)

9. In regard to claim 7, Garreau teaches:

- The method of claim 6 wherein selecting a remaining one of the plurality of output lines includes:
- modifying a second select signal; and
- selecting a remaining one of the plurality of output lines based on the modified second select signal.

(Note: col. 4, lines (57-67) through col. 5, lines (1-25) the Master controller detail description in Garreau)

10. In regard to claim 8, Garreau teaches:

- The method of claim 1 wherein:
- employing a remaining one of the plurality of input lines to receive the test signal for the processor includes:
- selecting a remaining one of the plurality of input lines; and
- employing the selected remaining one of the plurality of input lines to receive the test signal; and
- employing a remaining one of the plurality of output lines to send the test result from the processor includes:
- selecting a remaining one of the plurality of output lines; and
- employing the selected remaining one of the plurality of output lines to send the test result from the processor.

(Note: FIG. 4, reference characters (400) Programmable Switch in Garreau)

(Note: col. 6, lines (49-67) through col. 7, lines (1-28) in Garreau)

11. In regard to claim 9, Garreau teaches:

- The method of claim 8 wherein:
- selecting a remaining one of the plurality of input lines includes:
- modifying a first select signal; and

- selecting a remaining one of the plurality of input lines based on the modified first select signal; and
- selecting a remaining one of the plurality of output lines includes:
- modifying a second select signal; and
- selecting a remaining one of the plurality of output lines based on the modified second select signal.

(Note: col. 4, lines (57-67) through col. 5, lines (1-25) the Master controller detail description in Garreau)

12. In regard to claim 10, Garreau teaches:

- An apparatus for testing an IC comprising:
- a processor;
- a plurality of input lines coupled to the processor;
- a plurality of output lines Coupled to the processor; and
- a connector interface coupled to the plurality of input lines and the plurality of output lines;
- wherein the apparatus is adapted to:
- employ one of the plurality of input lines to receive a test signal for the processor;
- employ one of the plurality of output lines to send a test result from the processor; and
- if the test result is unsuccessful, perform at least one of:

- employing a remaining one of the plurality of input lines to receive the test signal for the processor; and
- employing a remaining one of the plurality of output lines to send the test result from the processor.

(Note: FIG. 6 and col. 7, lines (59-67) through col. 8, lines (1-12) in Garreau)

13. In regard to claim 11, Garreau teaches:

- The apparatus of claim 10 wherein the connector interface is adapted to apply the test signal to each of the plurality of input lines; and further comprising a first multiplexer coupled to the plurality of input lines and the processor, and adapted to:
- select one of the plurality of input lines; and
- receive the test signal for the processor on the selected input line.

(Note: col. 8, lines (29-48) in Garreau)

14. In regard to claim 12, Garreau teaches:

- The apparatus of claim 11wherein the first multiplexer is further adapted to:
- select a remaining one of the plurality of input lines; and employ the selected remaining one of the plurality of input lines to receive the test signal.

(Note: col. 8, lines (29-48) in Garreau)

15. In regard to claim 13, Garreau teaches:

- The apparatus of claim 11 further comprising a third multiplexer coupled to the connector interface and first multiplexer, and adapted to modify a first select signal, the first select signal corresponding to the first multiplexer; and
- wherein the first multiplexer is further adapted to select a remaining one of the plurality of input lines based on the modified first select signal.

(Note: col. 8, lines (29-48) in Garreau)

16. Claim 14 is rejected for the same reasons as per claim 11.

17. Claims 15 and 18 are rejected for the same reasons as per claim 12.

18. Claims 16 and 19 are rejected for the same reasons as per claim 13.

19. In regard to claim 17, Garreau teaches:

- The apparatus of claim 10 wherein the connector interface is adapted to apply the test signal to each of the plurality of input lines; and
- further comprising a first multiplexer coupled to the plurality of input lines and the processor, the first multiplexer adapted to:
- select one of the plurality of input lines; and
- receive the test signal for the processor from the selected input line;
- wherein the processor is further adapted to apply the test result to each of the plurality of output lines; and

- further comprising a second multiplexer coupled to the plurality of output lines and the connector interface, the second multiplexer adapted to:
- select one of the plurality of output lines; and send the test result from the processor using the selected output line.

(Note: FIG. 6 and col. 7, lines (59-67) through col. 8, lines (1-12) in Garreau)

(Note: col. 8, lines (29-48) in Garreau)

20. In regard to claim 20, Garreau teaches:

- The apparatus of claim 10 wherein the connector interface is adapted to couple to a service processor.

(Note: FIG. 8 in Garreau)

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Avery et al. US publication no. 2004/0193979 teaches circuit configurator arrangement and approach.
- Avery et al. US publication no. 2004/01939980 teaches circuit testing including configurable switch control for automatically detecting and routing test signals.
- Hashizume et al. patent number 5150044 teaches semiconductor IC comprising scan paths having individual controllable bypass.

- Mote, Jr. US patent 5805609 teaches method and apparatus for testing a megacell in an ASIC using JTAG.
- Whetsel US patent no. 6727722 teaches process of testing a semiconductor wafer of IC dies.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

Sam Rizk, MSEE, ABD

Examiner

ART UNIT 2133

9/13/06

GUY LAMARRE
PRIMARY EXAMINER